

Pushout with Virtual Thresholds Buffer Management Scheme in a Shared Buffer ATM Switch

Ruey-Bin Yang, Yuan-Sun Chu, Cheng-Shong Wu and Ming-Cheng Liang[†]

Department of Electrical Engineering
National Chung Cheng University

[†]Department of Electronic Engineering
I-Shou University

Author for correspondence: Ruey-Bin Yang

Address: 160, San-Hsing, Ming-Hsiung, Chia-Yi 621, Taiwan, R.O.C.

TEL: 886-5-272-0411 ext. 23257

Fax: 886-5-272-0862

E-mail: d8642009@ccunix.ccu.edu.tw or rueybinyang@giga.net.tw

Abstract- In this paper, we investigate the performance metrics of buffer management schemes. In general, the selective pushout (SP) scheme can support very low loss probability of the high priority cells, but it may cause the unfairness of buffer allocation among different output queues and high overall cell loss probability. In order to fit the dynamic required performance metrics of ATM switches, a novel buffer management scheme called pushout with virtual thresholds (PVT) is proposed. In the PVT scheme, each output queue is guaranteed to increase in length until its virtual threshold (VT). Simulation results show the PVT can dynamically achieve the fairness and low overall cell loss probability or very low loss probability of the high priority cells by adequately adjusting the VT. Specially, when the $VT = 0$, the PVT control can be viewed as the SP control.

Key words: pushout, virtual threshold, shared buffer, fairness

1. Introduction

Asynchronous transfer mode (ATM) is a technique adopted by ITU-T as the basis for Broadband ISDN. ATM is expected to be the transfer carrier for different data services such as video, voice and interactive data. Therefore, ATM must be capable of supporting different Quality of Service (QoS) requirements such as fairness, delay, jitter and cell loss rate. The allocation of buffer and buffer management schemes will directly affect the performance of an ATM switch. It was concluded that output queue and completely shared buffer schemes can achieve optimal throughput-delay performance [1]. The performance of the input queue is worst because of the head-on-line problem. Some methods [2] are proposed to solve this problem.

How to design an efficient buffer management scheme is also important for the switch performance. A proper buffer management scheme will not only support different cell loss priorities (CLP), but also provide the fairness and maximized overall throughput. To support different loss probabilities for various priority cells, the buffer control scheme will need to provide more much buffer space to the high priority (CLP=0) cells than the low priority (CLP=1) cells. To guarantee fairness, the buffer control scheme needs to fairly allocate the buffer among output ports. To maximize the overall throughput is the same as to minimize the overall cell loss probability. However, the performance metrics of buffer management policies might be contradictorily. For example, when a complete partitioning (CP) scheme is used, this scheme is fair but the overall cell loss probability is high due to lack of dynamic buffer adjustability to absorb the traffic burstiness.

Several buffer management schemes were proposed to reduce the overall cell loss probability and support fairness for network without priority considerations [3]-[6]. In order to investigate the effect of multiple CLP, two loss priority schemes, i.e., the partial buffer sharing (PBS) scheme and the pushout scheme are proposed. In the PBS scheme [7]-[10], a

static threshold T is assigned to the buffer. When the current queue length is smaller than T , all arrival cells are stored in the buffer. Once the queue length reaches T , only CLP=0 cells are admitted to enter the buffer.

In the use of pushout scheme [10]-[13], two different approaches are proposed. First, we consider the pushout scheme in a per port basis [13], i.e., an arrival CLP=0 cell could not be discarded if there exists at least one CLP=1 cells resided in the corresponding logical output queue. If there is no CLP=1 cell resided in the corresponding output queue, the CLP=0 cell will be dropped. Second, the pushout scheme is applied to the shared buffer in a whole buffer basis (or namely selective pushout (SP) [10]). In this case, when buffer is not full, all arrival cells are accepted. When buffer is full, the arrival CLP=0 cell could push out the CLP=1 cell nearest the head of the longest output queue. If there are no CLP=1 cells in the whole buffer, then the arrival CLP=0 cell pushes out the CLP=0 cell at the head of the longest queue. For the same rule, a CLP=1 cell arriving to a full buffer is also allowed to push out the CLP=1 cell nearest the head of the longest queue; if there are no CLP=1 cells in the whole buffer, the arrival CLP=1 cell is dropped. According to the discipline of SP, the SP approach can offer a very low loss probability of CLP=0 cells. However, the SP scheme may excessively push out the CLP=1 cells for non-overloaded output ports, so the fairness and overall cell loss probability might be degraded.

For dealing with these problems, we propose a buffer management scheme called pushout with virtual thresholds (PVT) in this paper. The PVT scheme is a modified version of the SP scheme. The difference is that the PVT is able to dynamically adjust the buffer allocation for different output queues. The key idea of PVT scheme is to allocate a virtual threshold VT_i for output queue i , by adjusting the VT_i , the PVT scheme virtually reserves the amount of VT_i buffer space for output queue i . The virtual reservation means there is no real reservation

of buffer space when the buffer is not full. When the buffer is full, then the amount of VT_i buffer space is guaranteed for output queue i to increase in length.

The paper is organized as follows. In Sect. 2, the operation of PVT scheme is described. In Sect. 3, we show the system model in our simulations. The system model is divided into two parts. We introduce the switch architecture in Sect. 3.1 and the input traffic model in Sect. 3.2. In Sect. 4, numerical simulation results of PVT scheme under different traffic conditions are presented. Finally, the conclusions and future works appear in Sect. 5.

2. Pushout with Virtual Thresholds Scheme

In this section, we describe the operation of the PVT scheme. The PVT scheme can be viewed as the combination of the threshold and the SP mechanisms. First, we introduce how to determine the value of VT . The value of VT is decided according to the performance requirement of the fairness and low overall cell loss probability or very low loss probability of CLP=0 cells. If the system providers would like to provide the fairness and low overall cell loss probability in ATM switches, larger value of VT may be required. Inversely, if the very low loss probability of CLP=0 cells is preferred, smaller value of VT may be required. In later section, we will show the effect of different value of VT . As follows, we introduce the details of the PVT scheme.

Case 1: When buffer is not full

All the new arrival cells are admitted to enter the shared buffer without blocking.

Case 2: When buffer is full

An arrival CLP=0 cell could push out the CLP=1 cell nearest the head of the longest output queue with queue length larger than its VT . If there is no CLP=1 cell in this case, then

the arrival CLP=0 cell pushes out the CLP=0 cell nearest the head of the longest queue. If the arrival CLP=0 cell destined to the longest queue, the arrival CLP=0 cell is just discarded.

When the queue length of an arrival CLP=1 cell is smaller than its VT , the arrival CLP=1 cell will push out the CLP=1 cell nearest the head of the longest queue with queue length larger than its VT . If there is no CLP=1 cell in this case, then the arrival CLP=1 cell will push out the CLP=0 cell nearest the head of the longest queue. When the queue length of an arrival CLP=1 cell is larger than its VT , the arrival CLP=1 cell will push out the CLP=1 cell nearest the head of the longest queue with queue length larger than its VT . If there is no CLP=1 cell in this case, then the arrival CLP=1 cell is just discarded.

3. System Model

In this section, we show the system model in our simulation. The system model is divided into two parts. First, we introduce the switch architecture in Sect. 3.1. Second, the input traffic model is showed in Sect. 3.2.

3.1 Switch Architecture

Consider the architecture of a shared buffer ATM switch as depicted in Fig. 1. This ATM switch has N input ports, N output ports, and all output ports share a common buffer that is sufficient to accommodate B cells. Cells arrive from the input ports, go through the switch fabric, join their destination output queue in the shared buffer, then departure from their output queues according to first come first service (FCFS) discipline. Assume the transition probability that from input port i to output port j is denoted by $P_{i,j}$, we have

$$\sum_{j=1}^N P_{i,j} = 1 \quad i = 1,2,3,\dots,N \quad \dots\dots\dots (1)$$

3.2 Traffic Model

In order to emulate the real traffic, we use an “ON-OFF” source traffic model depicted in Fig. 2. The source traffic model consists of two states, one is “ON” state and the other is “OFF” state. The duration of the “ON” state and “OFF” state are both geometrically distributions with parameter P_{on-off} and P_{off-on} respectively. P_{on-off} represents the transition probability from “ON” state to “OFF” state and P_{off-on} represents the transition probability from “OFF” state to “ON” state. If the system stays in “ON” state, one cell is generated; otherwise, no cell is generated. Given the P_{on-off} and P_{off-on} , we can determine the mean burst length of “ON” state L_{on-off} , the mean burst length of “OFF” state L_{off-on} and the input traffic load ρ as follows:

$$L_{on-off} = \sum_{k=1}^{\infty} k \cdot P_{on-off} \cdot (1 - P_{on-off})^{k-1} = 1 / P_{on-off}$$

$$L_{off-on} = \sum_{k=1}^{\infty} k \cdot P_{off-on} \cdot (1 - P_{off-on})^{k-1} = 1 / P_{off-on}$$

$$\rho = \frac{L_{on-off}}{L_{on-off} + L_{off-on}} \quad (2)$$

Each source produces both CLP=1 cells at an average rate of ρ_1 and CLP=0 cells at an average rate of ρ_2 , where $\rho_1 + \rho_2 = \rho$. We adopt the mode which each burst is comprised of cells of only one priority; a given burst has CLP=1 cell with probability ρ_1 / ρ or CLP=0 cell with probability ρ_2 / ρ .

4. Numerical Results

In this section, we show the simulation results of the PVT scheme for a shared buffer ATM switch with 16x16 ports and the total buffer size is 256 cells. For simplicity, the equal size of

VT is applied to all output ports. The output ports are classified into two different types: overloaded and non-overloaded output ports according to their mean offered loads. The mean offered load of all overloaded output ports is set at the same value, denoted by OP , and the mean offered load of all non-overloaded output ports is also set at the same value, denoted by NOP . Thus, the mean offered loads of 16 output ports can be expressed as $TC [OP*m, NOP*n]$, where $m+n=16$. For example, $TC [0.995*8, 0.235*8]$ means that there are 8 overloaded output ports with $OP=0.995$ and 8 non-overloaded output ports with $NOP=0.235$.

In Fig. 3, we discuss the performance metrics of PVT scheme under $TC [0.9957*8, 0.7468*8]$ and $L_{on-off} = 20$. Besides, we assume all cells destined to the overloaded output ports are $CLP=0$ cells and all cells destined to non-overloaded output ports are $CLP=1$ cells. When the $VT = 0$, the overall cell loss probability is very high. Because of the $CLP=1$ cells of non-overloaded output ports are pushed out by the $CLP=0$ cells of overloaded output ports even if the output port is idle, the overall throughput will be largely decreased. In this case, the overall cell loss probability is very high.

When the value of VT is larger than 8, the overall cell loss probability is the lowest. Because of the throughput of each non-overloaded output port is protected. The loss probability of $CLP=0$ cells is kept the same value no matter which VT is, because of the long-term congestion. As for the fairness, by increasing the VT , we can guarantee the buffer space for the non-overloaded output ports. When the VT is set at 16, the allocation of buffer size is very fair ($256/16=16$ cells).

In Fig. 4, we discuss the PVT scheme under $TC [1.2446*1, 0.7468*15]$ and the other traffic conditions are the same as Fig. 3. In Fig. 4, the behavior is similar to the Fig. 3. From Fig.3 and Fig.4, when the $VT = 16$, the fairness, low overall cell loss probability and low loss probability of $CLP=0$ cells can be supported. It means the PVT scheme can largely improve

the unfairness and high overall cell loss probability of SP scheme.

In Fig. 5, we discuss the PVT scheme under TC $[0.9957*1, 0.7468*15]$ and $L_{on-off} = 20$. Besides, we also assume each arrival cell to be a CLP=1 cell with probability 0.1. No CLP=0 cell destined to non-overloaded ports is discarded, because of the CLP=0 cells destined to the non-overloaded ports belong to the shorter queue length with high priority. The loss probability of CLP=0 cells destined to overloaded port is stable when the value of VT is larger than 8. Because the queue length of non-overloaded ports often does not occupy larger than 8 cells in the shared buffer. As for the loss probability of CLP=1 cells destined to non-overloaded ports decreases when the value of VT increases. It means more much buffer space is allocated for the CLP=1 cells of non-overloaded output ports, so the CLP=1 cells could not be pushed out by the CLP=0 cells of overloaded output ports. Lastly, the loss probability of CLP=1 cells of the overloaded ports is very high, because these cells belong to the long queue with low priority. Obviously, the overall cell loss probability is dominated by the loss probability of CLP=1 cells of the overloaded output ports, so both of them have the approximate cell loss probability.

In Fig. 6, we assume $\rho_1/\rho = 0.05$ for the overloaded output ports and $\rho_1/\rho = 0.5$ for non-overloaded output ports. The other traffic conditions are the same as Fig. 5. When the value of VT increases, the loss probability of CLP=0 cells increases more quick than that of Fig. 5. Because of the loading of CLP=1 cells of overloaded output ports is decreased from 0.1 to 0.05, the ability of CLP=0 cells for overloaded output ports to push out the CLP=1 cells of non-overloaded output ports is important to improve the loss of CLP=0 cells. So the loss probability of CLP=0 cells for overloaded ports increases quickly.

From Fig. 5 and Fig. 6, the very low loss probability of CLP=0 cells is hold at the $VT = 0$, but the high throughput and the fairness are hold at the $VT = 16$. Therefore, we only discuss

the $VT = 0$ and $VT = 16$ to see how robust the performance metrics of the PVT scheme. In Fig. 7, we change the number of overloaded output ports. The loading of overloaded output ports is 0.9957 and loading of non-overloaded output ports is 0.7468. In Fig. 8, we discuss the effect of burstiness and the other traffic conditions are the same as Fig. 6. In Fig. 7 and Fig. 8, the PVT scheme still provide very low loss probability of CLP=0 cells at $VT = 0$. If the fairness and low overall cell loss probability is required, the value of VT is set at 16. By using the PVT scheme, the network provider can dynamically adjust the value of VT to satisfy the required performance metrics or to maximize the revenue according some pricing models.

5. Conclusions

This paper proposes a novel buffer management scheme called pushout with virtual threshold (PVT) to deal with the performance metrics regarding the fairness, the overall throughput and the loss probability of CLP=0 cells. In our simulation results, if the fairness and high overall throughput is preferred, the adequate value of VT is set at 16. Otherwise, if the very low loss probability of CLP=0 cells is preferred, the adequate value of VT is set at 0. In our future works, we would like to apply the PVT scheme to the packet switches. We also want to establish a pricing model and find the optimal value of VT with maximum revenue.

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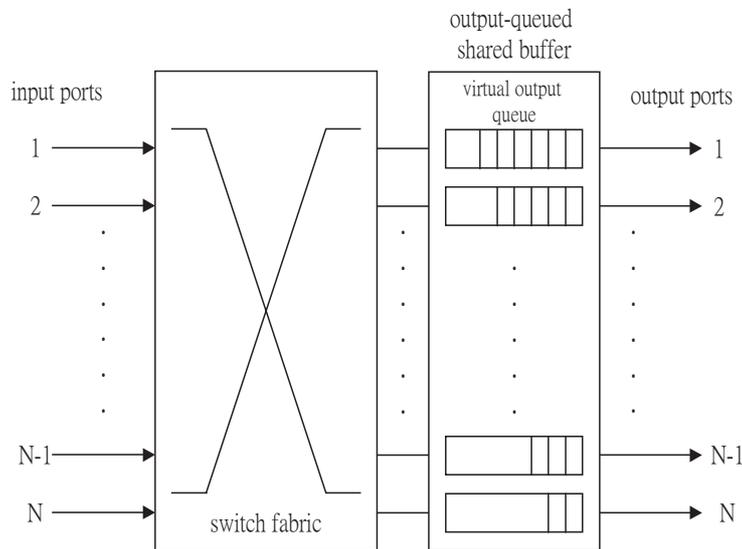


Fig. 1 The architecture of an $N \times N$ output-queued shared buffer ATM switch

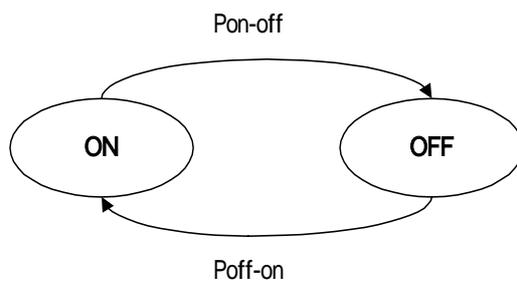


Fig. 2 "ON-OFF" input traffic model

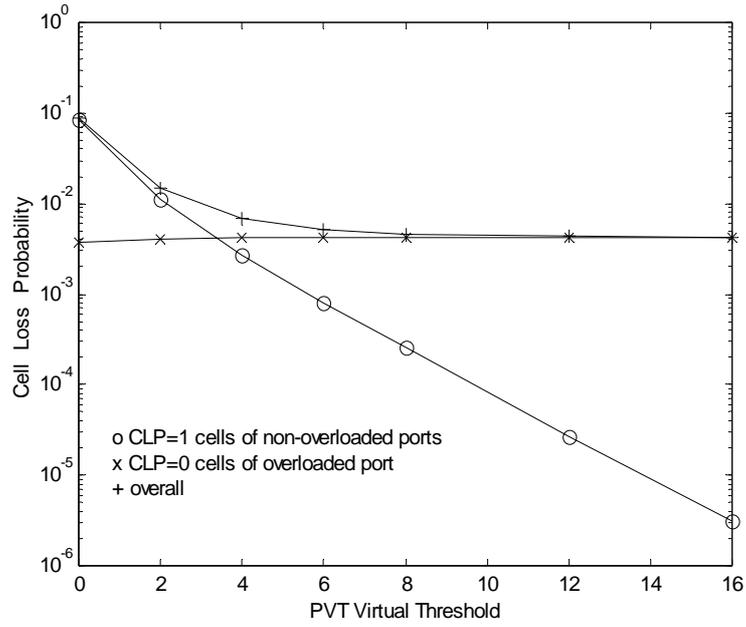


Fig. 3 Cell loss probability vs. PVT virtual threshold under TC [0.9957*8, 0.7468*8]

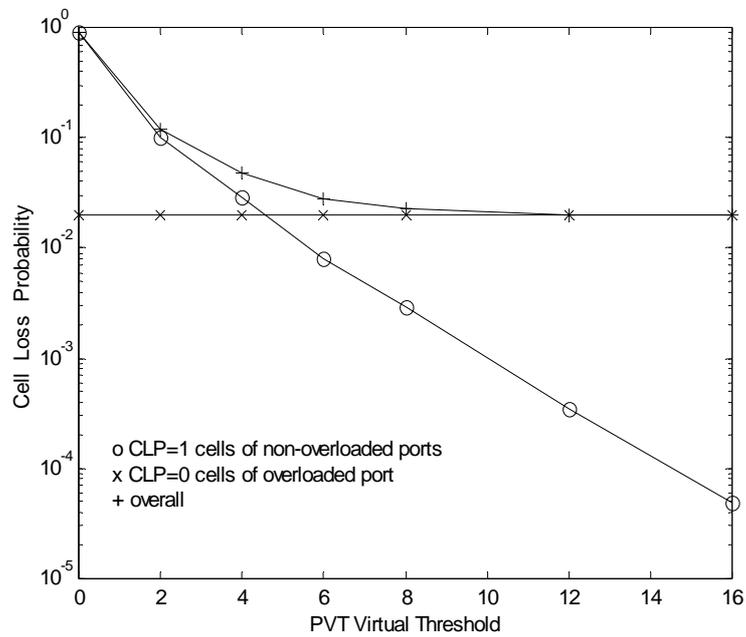


Fig. 4 Cell loss probability vs. PVT virtual threshold under TC [1.2446*1, 0.7468*15]

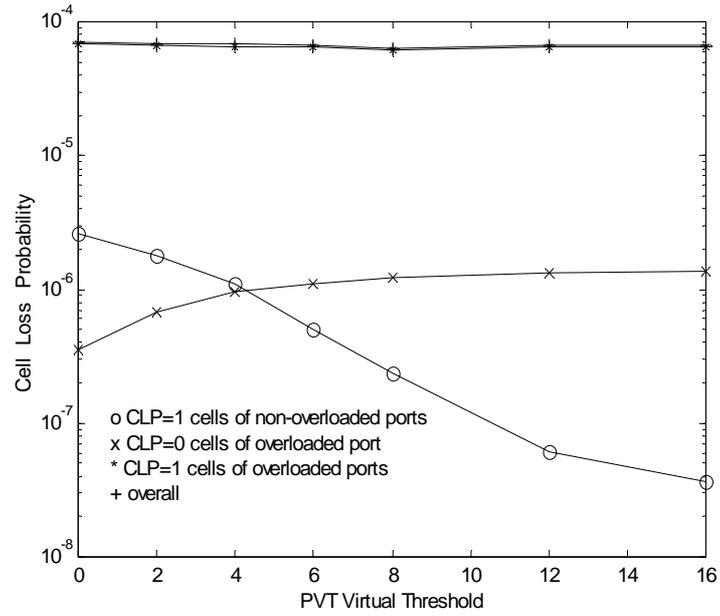


Fig. 5 Cell loss probability vs. PVT virtual threshold under TC [0.9957*1,0.7468*15]

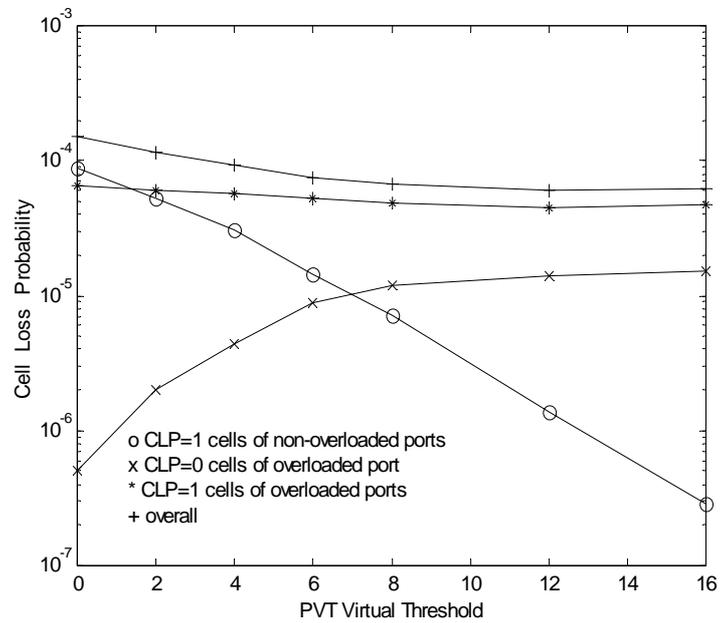


Fig. 6 Cell loss probability vs. PVT virtual threshold under TC [0.9957*1,0.7468*15]

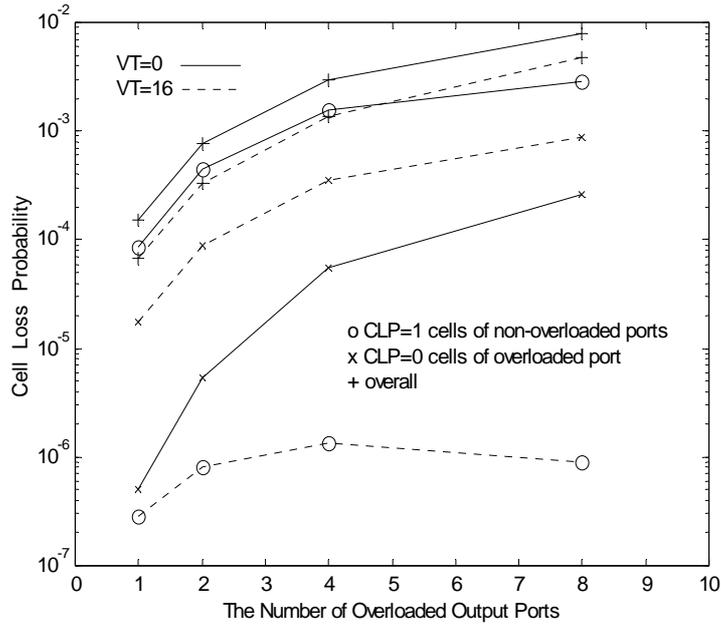


Fig. 7 Cell loss probability vs. PVT under various numbers of overloaded ports

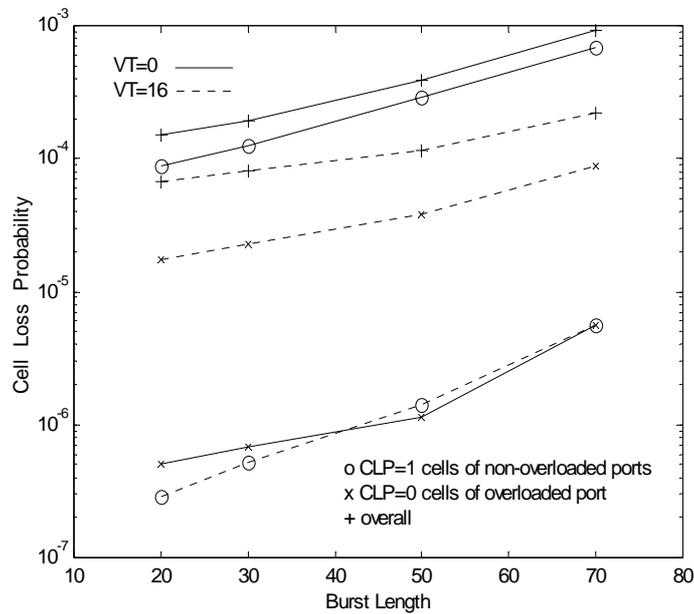


Fig. 8 Cell loss probability vs. PVT under various burst lengths under

TC [0.9957*1,0.7468*15]