A Dual-Polarity High Voltage Generator for FLASH Memories Using Two-Phase Clocking *

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Abstract

A novel voltage generator using 4 clocks with two different phases is presented in this work to provide a high voltage supply required by FLASH memories during programming mode and erase mode operations. Both the positive and negative polarities of the voltage are generated to serve as the programming voltage and the erase voltage, respectively. The proposed design is carried out by gated pass transistors and switched capacitors. The regulated generated voltages which the proposed design can provide is +11.7 V and -11.6 V given VDD = 2.5 V when the circuit is implemented by TSMC 0.25 μm 1P5M CMOS technology. The maximum power dissipation is estimated to be 3.8 mW given 12.5 MHz clocks.

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1 Introduction

The evolution toward modern low-power computer systems demand that memories regardless of volatile or non-volatile must work in a low-voltage power supply. The supplied voltage provided by the power of the system could be as low as one volt which might either slow down the read/write operations of the memories or generates fatal errors. Neither of these scenarios is acceptable. Charge pumps play an important role in high voltage generators (HVG) for memories to resolve such a problem. For instance, non-volatile memories, e.g., FLASH and EEPROM, requires high voltages for programming and erasing (typically $\approx \pm$ 12 V) [7], [8]. By contrast, ultra low-voltage volatile memories, e.g., DRAM and SRAM, also demand boosted voltage generators (BVG) to compensate the threshold voltage of the MOS or boosting bit line voltage to raise the speed of readout operations [2], [3], [5]. Owing to the presence of the threshold leakage and the body effect of MOS transistors, the pumping gain of prior charge pump designs has been a problem to be resolved. It is particularly crucial when the EEPROM or FLASH is integrated with CMOS circuits in SOC (system-on-chip) designs. Most of the prior works were focused on the generation of a positive high voltage [2], [3], [4], [5], [8]. However, a negative high voltage is often needed in the erase mode of the non-volatile memories or in the read operations of the volatile memories. Another important application of high negative voltages is the back bias which is used to reduce the subthreshold current and junction capacitance. The negative voltages produced by a back bias generator (BBG) can be used to enhance the device isolation capability and the latch-up immunity. In this paper, we present an improved Dickson charge pump design, [1], [6], which utilizes gated pass transistors and switched capacitors, to generate both positive and negative voltages which are large enough to serve as the programming voltage and erase voltage for flash memories. The highest output voltage is around $\pm$12 volts, given that the VDD = 2.5V.

2 High Voltage Generator

The maximum ideal output voltage, $N\cdot$ VDD, is never achieved for a typical Dickson's charge pump design [6] because of parasitic capacitors, non-zero threshold voltages, and body effect. The number of the stages must be increased to compensate these factors. Otherwise, techniques which reduce V_{thn} must be adopted to alleviate the increase of stages, including floating substrate to reduce the V_{thn} or boost the gate drive of the NMOS transistor at each stage. These methods depend whether the process provides deep N-well layer or not.

2.1 Architecture of the proposed HVG

Multi-phase clocking schemes show another alternative to resolve the design for high voltage generators, e.g., [7]. However, the non-zero V_{thn} drop unavoidably results in the large number of pumping stages. We propose to add a built-in high voltage source which supplies a voltage $\geq$ VDD+V_{thn} to cross out the unwanted voltage drops when necessary. The entire proposed design is summarized in Fig. 1, including a ring oscillator, a clock generator, a high voltage source, buffers, output regulator, and a charge pump.

clock generator : Two pairs of out-of-phase clocks with normal voltage swing are generated, e.g., CLK1$'$, CLK2$'$, CLK3$'$, and CLK4$'$, based on the clock generated by the ring oscillator.

high voltage source : The non-zero V_{th} is the key reason why the prior charge pumps suffered. Hence, the gate drive applied to the pass transistors must be boosted to be at least larger than VDD+V_{th}, preferably 2$\cdot$VDD. The output of this module is defined to be VDD2 which is 2$\cdot$VDD - V_{thn}.

buffers : Besides buffering the mentioned four clock signals, the buffers module also generate their individual complementary clock signals. Hence, the number of clocks fed into the charge pump is a total of eight. Notably, the power supply of the buffers to generate CLK1, $\overline{\text{CLK1}}$, CLK3, and $\overline{\text{CLK3}}$ are connected to VDD2 supplied by the high

voltage source module instead of the common VDD. Hence, the swing of these fours clocks is between VDD2 and GND.

charge pump : This module contains one set of cascaded PMOS pass transistors which are driven by the complementary of the mentioned four clocks, namely, $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, $\overline{\text{CLK3}}$, and $\overline{\text{CLK4}}$, to generate a negative high voltage which is V_{out-}. On the other hand, it also contains another set of cascaded NMOS pass transistors which are driven by the mentioned four clocks, i.e., CLK1, CLK2, CLK3, and CLK4, to generate a positive high voltage which is V_{out+}.

regulator : The function of this module is to detect the steady state of the output voltages. It possesses a voltage comparator to detect whether V_{out+} is larger than a predetermined ratio of a V_{ref}. If the condition is met, an EN=0 will be signaled to the ring oscillator to disable the oscillation to lock the output voltages.

2.2 Basic operations of charge pumps

The core of the proposed HVG is the charge pump driven by two-phase clocking. The set of the cascaded PMOS pass transistors to produce a high negative voltage is shown in Fig. 2. Notably, each of the PMOS transistors is driven by one of $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, $\overline{\text{CLK3}}$, and $\overline{\text{CLK4}}$ according to the arrangement in Fig. 2. In short, $\overline{\text{CLK1}}$ drives P2, P6, P10; $\overline{\text{CLK2}}$ drives P1, P5, P9; $\overline{\text{CLK3}}$ drives P4, P8, P12; $\overline{\text{CLK4}}$ drives P3, P7, P11. Fig. 3 reveals the waveforms of the four clocks applied to the PMOS transistors. The operations are described as follows.

initial state : Since all of the clocks have the same period, the state of the charge pump are recycled. Hence, the initial state before t_0 in Fig. 3 is identical to that at t_{15}.

t_0 **to** t_4 **:** $\overline{\text{CLK1}}$ and $\overline{\text{CLK4}}$ stay low, while $\overline{\text{CLK3}}$ is kept high (VDD2 $\approx$ 4.0 V) and $\overline{\text{CLK2}}$ is VDD. P3 is turned on. $\overline{\text{CLK1}}$ in fact change from VDD2 at the initial state to GND = 0 V, which indicate a -VDD2 gate drive is applied at the gate of P2. It, thus, leads to the reduction of the threshold voltage, i.e., V_{thp} of P2 $\approx$ 0 V. Then, the GND signal at the drain of P2 is propagated to C_{P2}.

t_5 **:** A low to high transition occurs in $\overline{\text{CLK1}}$ which turns off P2 such that C_{P2} is isolated from the leftmost GND signal.

t_6 **:** A high to low transition of $\overline{\text{CLK2}}$ appears. The polarity of the voltage at C_{P2}, thus, is changed oppositely to be -VDD. In the mean time, owing to the steady low state of $\overline{\text{CLK4}}$, the negative voltage is applied to the gate of P4.

t_7 **:** $\overline{\text{CLK4}}$ remains at VDD to shutdown P3 such that the isolation of gate drive of P4 is preserved.

t_8 **to** t_{12} **:** $\overline{\text{CLK3}}$ drops from VDD2 to GND which makes the gate drive of P4 is "more" negative than the voltage at C_{P2}. P4, thus, is turned on with a ≈ 0 V threshold voltage drop. The negative voltage of C_{P2} is then propagated to C_{P4}.

t_{13} **:** $\overline{\text{CLK3}}$ returns from GND to VDD2. P4 is off. The voltage of C_{P4} is isolated and kept to be -VDD.

t_{14} **:** $\overline{\text{CLK4}}$ drops to GND to accumulate the negative voltage at C_{P4} to be 2×(-VDD).

t_{15} **:** $\overline{\text{CLK2}}$ returns from GND to VDD to restore the initial state of the entire pumping cycle.

It can be concluded that every stage, which is composed of two PMOS pass transistors and two capacitors, can add another -VDD to the final output. Notably, C_{out-} is used as a lowpass filter while the self-saturated P13 is basically a diode to rectify the output waveform. By the same design methodology, a positive charge pump is given in Fig. 4 which is driven by the other clock signal set, i.e., CLK1, CLK2, CLK3, and CLK4, which is extactly out-of-phase w.r.t. those in Fig. 3.

2.3 Schematics of HVG modules

clock generator : The output of the oscillator is used to generate two pairs of out-of-phase clocks with VDD swing.

high voltage source : The major function of this module is to produce a voltage at least larger than VDD+V_{thn}, preferably 2·VDD. The schematic is shown in Fig. 5. When

the input OSC_OUT is low, M91 is a diode to pull up node F91 to VDD-V_{thn}. As soon as OSC_OUT turns high, charge accumulation effct via C91 forces F91 to be boosted to VDD+VDD-V_{thn} = 2·VDD-V_{thn}. F91, thus, turns on M95 and M94 such that node F92 and F93 are pulled up close to VDD. Meanwhile, node F94 stays in VDD at the same time. Hence, the total voltage of node F92 and F93 will become 2·VDD which propagtes via M96 to produce the final output voltage close to 2·VDD-V_{thn}.

regulator : An ideal voltage output for generators should be regulated to reach the goal of low dropout. Fig. 6 shows the regulator in the proposed design. Input A recieves the initialization input. The output EN is fed back to the enable control of the ring oscillator to determine whether the ring oscillator is enabled or not. V_{in} is coupled to the positive generated voltage of the charge pump module. The operation is summarized as follows.

$V+ < V_{ref}$: The comparator signals a 0 which in turn pulls up EN to enable the ring oscillator.

$V+ > V_{ref}$: If V_{in} is gradually increased to be larger than the reference voltage, V_{ref}, EN becomes low to disable the oscillator such that V_{in} is locked in a steady state. The V_{ref} can be realized by a traditional bandgap design to meet the requirement : $V_{in} = V_{ref} \cdot \frac{C_{r1}+C_{r2}}{C_{r1}}$.

3 Simulation and Implementation

The proposed design is carried out by using TSMC 0.25 μm 1P5M CMOS process in CADENCE EDA tools. Fig. 7 shows the layout of the entire HVG. Post-layout simulation results (with the regulator) are shown in Fig. 8. The performance of two prior designs, Lin's [4], and Dickson's [6], are also presented in the same figure. The comparison are based upon 4 pumping stages, VDD=2.5V, 25^{o}C, and TT transistor models. Regardless of generating positive or negative voltages, our proposed design provides a better result. The features of the proposed HVG chip is summarized as Table 1.

Fig. 9 shows the comparison of Lin's [4], Dickson's [6], and the proposed design given the same four pumping stages without any regulator. Fig. 10 summarizes the overall

VDD	2.5V
VOUT+	+11.7V
VOUT-	-11.6V
power dissipation	3.8 mW @ 12.5 MHz
transistor count	436 (plus 2 res and 27 cap)
area	954.2×908.2 μm^2

Table 1: The characteristics of the HVG chip (25^oC, TT models, with the regulator)

performance of these three designs when the input voltage (VDD) is varied from 1.5 V to 3.5 V. Besides, Fig. 11 illustrates the output voltages of the three designs when the number of pumping stages increased from 4 to 8. All of these comparisons conclude that the proposed design is able to generate the highest voltages regardless the polarities given the same testing condition.

4 Conclusion

In this paper, a novel dual-polarity HVG design, which utilizes only pass transistors and switched capacitors, is presented to generate both positive and negative high voltages to serve as programming and erase voltages of FLASH memory devices.

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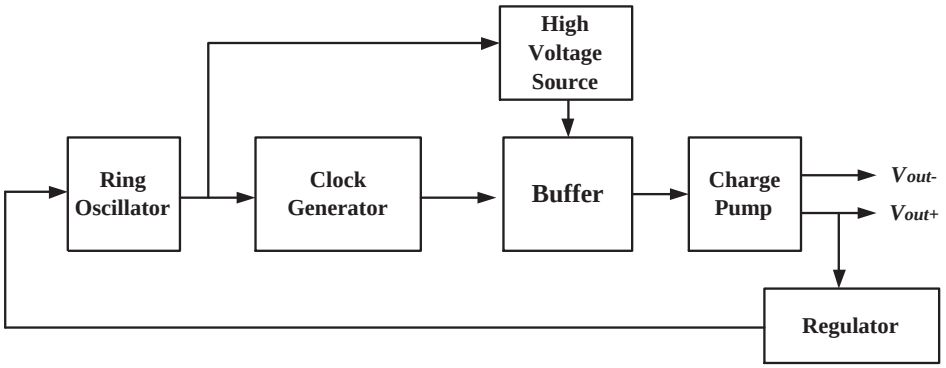

Figure 1: Block diagram of the proposed charge pump

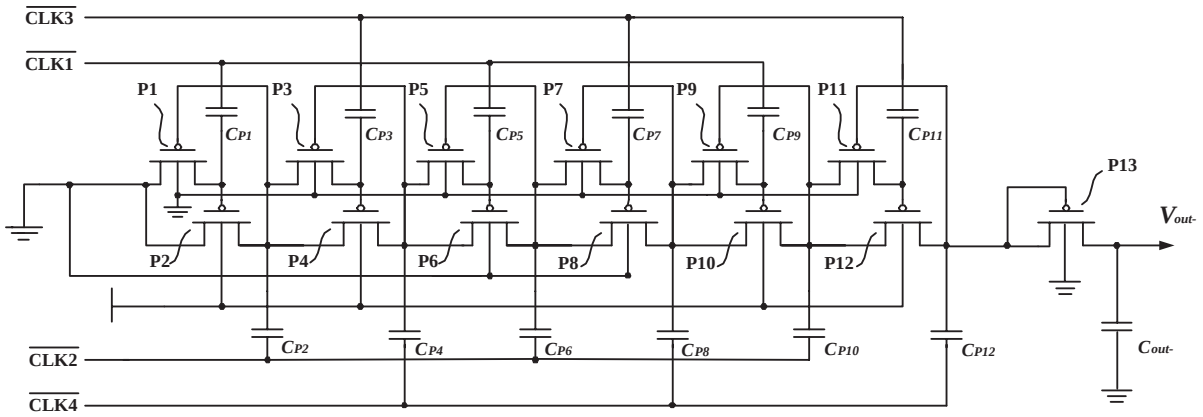

Figure 2: Negative voltage charge pump

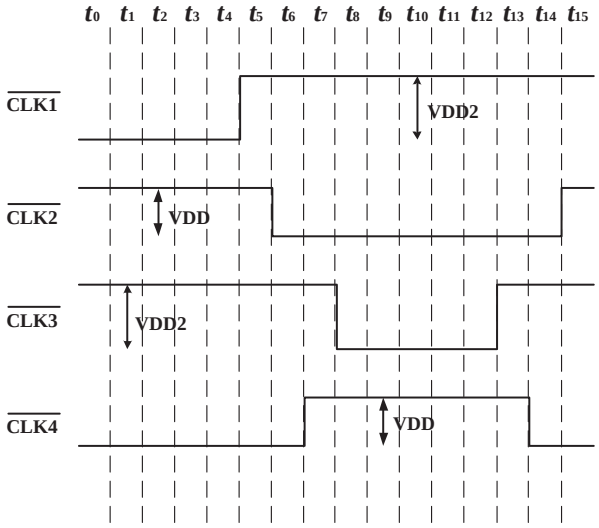

Figure 3: Clocks to drive the negative voltage charge pump

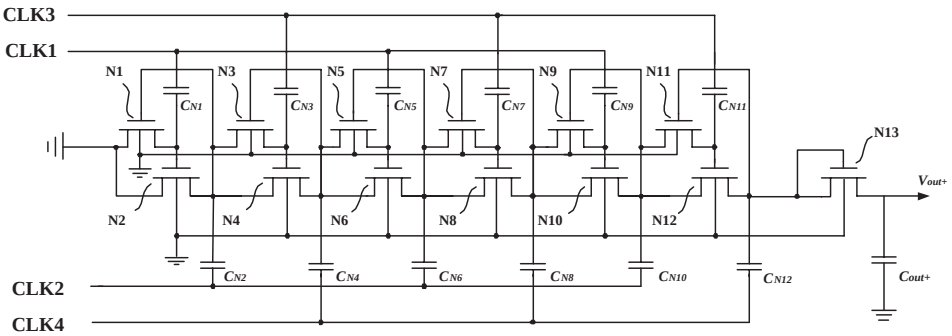

Figure 4: Positive voltage charge pump

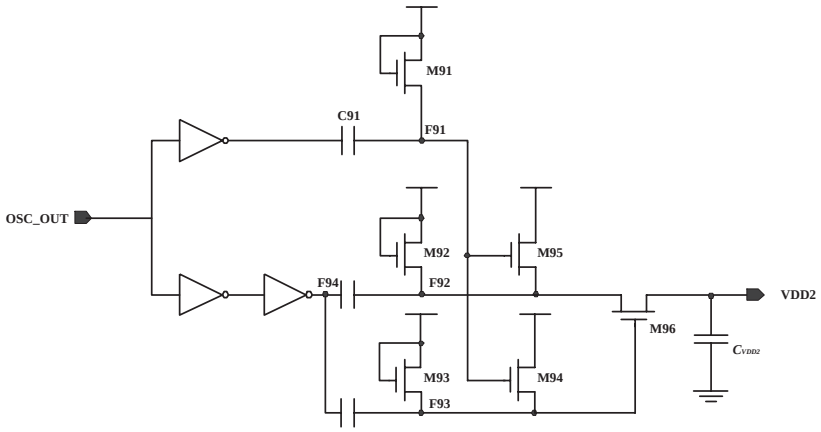

Figure 5: High voltage source

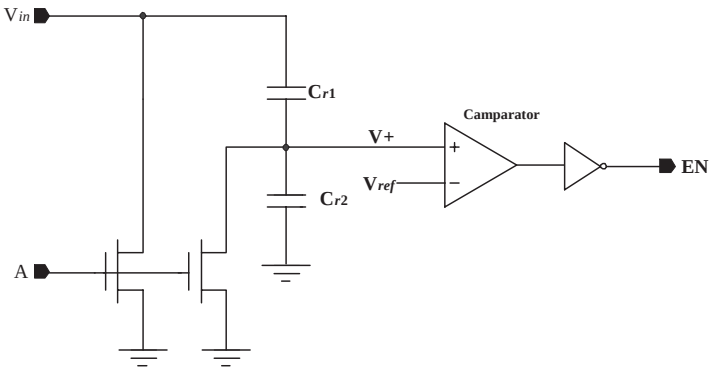

Figure 6: Regulator schematic

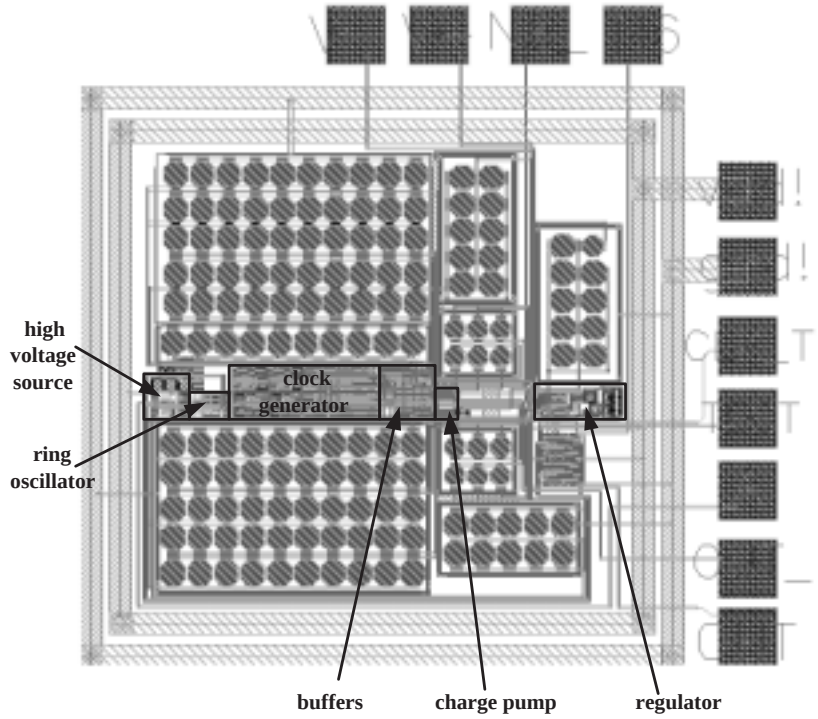

Figure 7: Chip layout

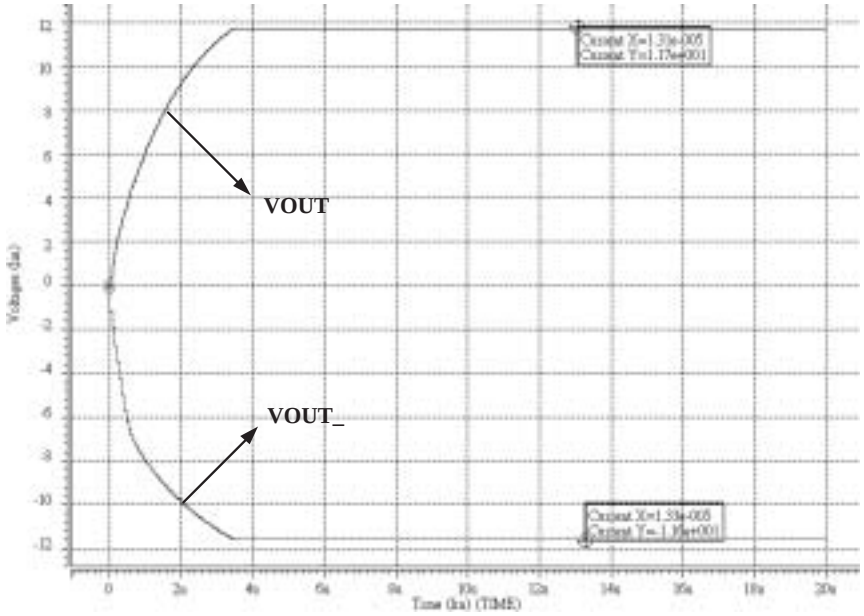

Figure 8: Post-layout simulation (with the regulator)

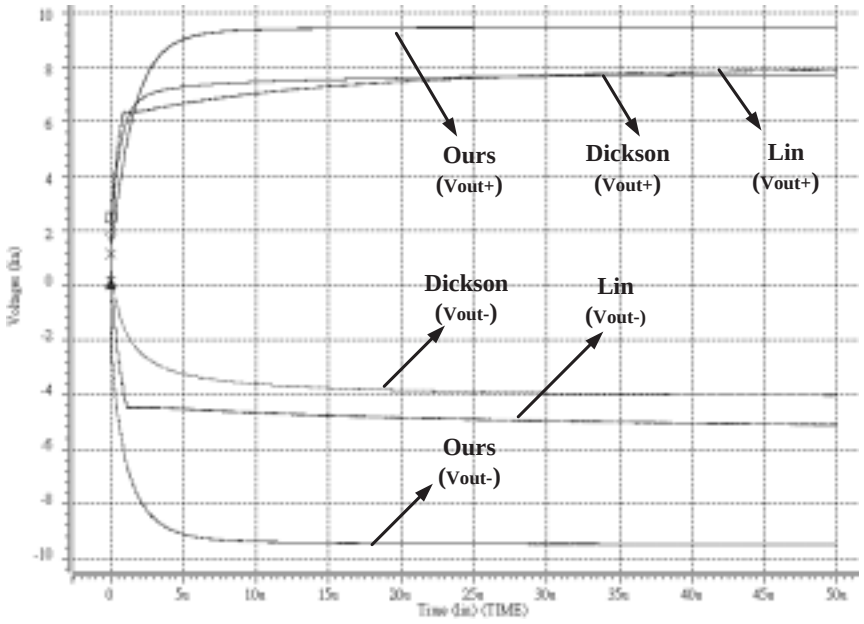

Figure 9: Comparison with the prior designs

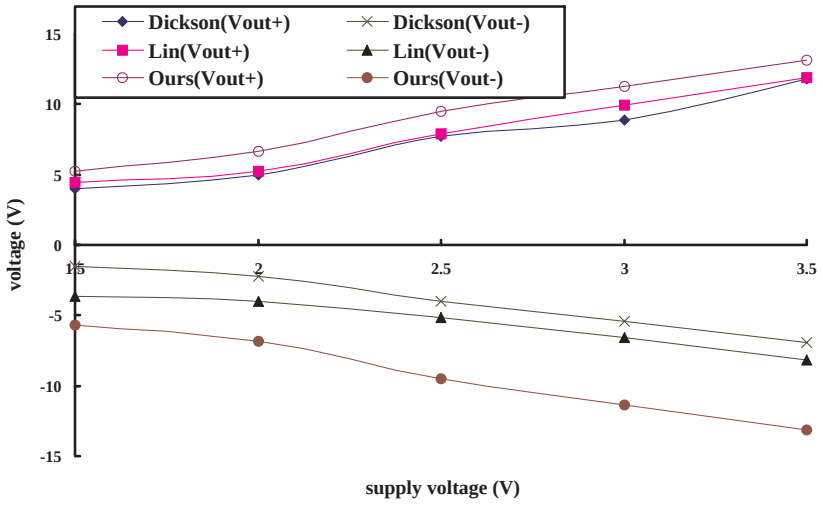

Figure 10: Comparison with the prior designs given the same input

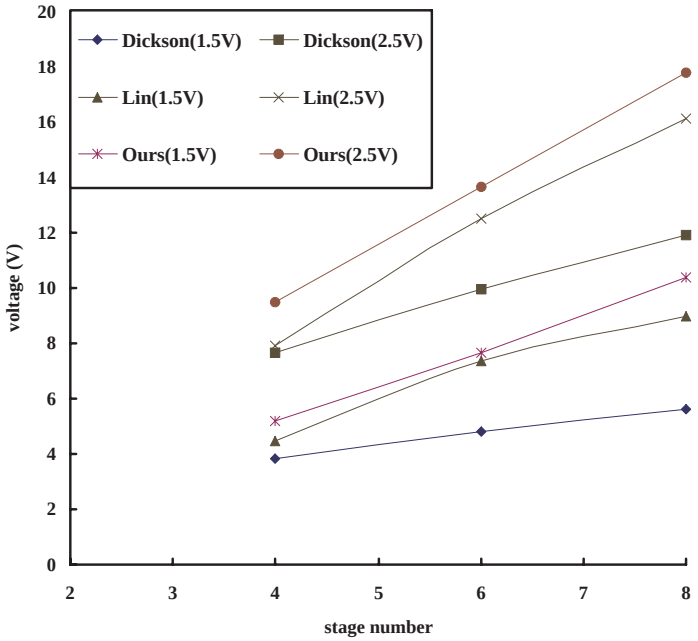

Figure 11: Comparison with the prior designs given the same stages